Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): A method comprising:

supplying a negative voltage to at least one deselected wordline of a memory array from a decoder coupled to the at least one deselected wordline; and

providing the negative voltage and a control negative voltage to the decoder.

Claim 2 (original): The method of claim 1, further comprising supplying a positive voltage to a selected wordline of the memory array to program the selected wordline while supplying the negative voltage.

Claim 3 (original): The method of claim 2, further comprising supplying the negative voltage to all wordlines of the memory array except the selected wordline.

Claim 4 (original): The method of claim 2, further comprising providing a second positive voltage signal to a selected bitline of the memory array.

Claim 5 (original): The method of claim 4, further comprising reducing a leakage current through at least one deselected cell coupled to the selected bitline of the memory array.

Claim 6 (cancel)

Claim 7 (currently amended): The method of claim [[6]] 1, further comprising providing the control negative voltage to a substrate of a transistor of the decoder coupled to pass the negative voltage to the at least one deselected wordline.

Claim 8 (cancel)

Claim 9 (currently amended): The method of claim 1, further comprising supplying the negative voltage to the deselected wordline during a first time period, and supplying a positive voltage to the same wordline during a second time period to program at least one memory ~~cells~~ cell coupled thereto.

Claim 10 (currently amended): An apparatus comprising:

a decoder to supply a negative voltage to a deselected address line of a memory array, the decoder comprising a first transistor coupled to receive a negative control voltage and the negative voltage and to pass the negative voltage to the deselected address line.

Claim 11 (original): The apparatus of claim 10, wherein the decoder is further coupled to supply a positive voltage to the same address line if it is selected to be programmed.

Claim 12 (cancel)

Claim 13 (currently amended): The apparatus of claim [[12]] 10, further comprising a second transistor coupled to the first transistor and the deselected address line to pass a program pulse to the deselected address line if it becomes a selected address line.

Claim 14 (currently amended): The apparatus of claim [[12]] 10, further comprising a pre-driver circuit to disable the first transistor if the deselected address line becomes a selected address line.

Claim 15 (original): The apparatus of claim 10, further comprising a plurality of memory cells coupled to the decoder via the deselected address line.

Claim 16 (original): The apparatus of claim 15, wherein the plurality of memory cells comprise multi-level cells of a flash memory.

Claim 17 (currently amended): An article comprising a machine-readable storage medium containing instructions that if executed enable a system to:

supply a negative voltage to at least one deselected wordline of a memory array; and

provide a negative control voltage to a substrate of a transistor coupled to pass the negative voltage to the at least one deselected wordline.

Claim 18 (original): The article of claim 17, further comprising instructions that if executed enable the system to supply a positive voltage to a selected wordline of the memory array to program the selected wordline while the negative voltage is supplied to the at least one deselected wordline.

Claim 19 (original): The article of claim 18, further comprising instructions that if executed enable the system to supply the negative voltage to all wordlines of the memory array except the selected wordline.

Claim 20 (cancel)

Claim 21 (cancel)

Claim 22 (currently amended): A system comprising:

a memory array having a plurality of memory cells each coupled to a wordline and a bitline;

a decoder coupled to the memory array to supply a negative voltage to a deselected wordline of the memory array, wherein the decoder comprises a first transistor to pass the negative voltage to the deselected wordline and a second transistor coupled to the first transistor to pass a program voltage, if the deselected wordline becomes a selected wordline; and

a wireless interface coupled to the memory array.

Claim 23 (original): The system of claim 22, wherein the decoder is further coupled to supply a positive voltage to the deselected wordline if it becomes a selected wordline.

Claim 24 (original): The system of claim 22, further comprising a second decoder to supply a positive voltage to a selected wordline while the negative voltage is supplied to the deselected wordline.

Claim 25 (currently amended): The system of claim 22, wherein ~~the decoder comprises a~~ the first transistor ~~having~~ comprises a well coupled to receive a negative control voltage, a source terminal coupled to receive the negative voltage, and a drain terminal coupled to pass the negative voltage to the deselected wordline.

Claim 26 (cancel)

Claim 27 (currently amended): The system of claim [[25]] 22, further comprising a pre-driver circuit to disable the first transistor if the deselected wordline becomes a selected wordline.

Claim 28 (original): The system of claim 22, wherein the memory array comprises a flash memory.

Claim 29 (original): The system of claim 28, wherein the flash memory comprises a multi-level cell flash memory.

Claim 30 (original): The system of claim 22, wherein the wireless interface comprises an antenna.

Claim 31 (new): The apparatus of claim 10, wherein the first transistor comprises a well coupled to receive the negative control voltage, a source terminal coupled to receive the negative voltage, and a drain terminal coupled to pass the negative voltage to the deselected address line.

Claim 32 (new): The system of claim 22, further comprising a negative switch coupled to provide the negative voltage and a negative control voltage to the decoder.

Claim 33 (new): The system of claim 32, wherein the negative switch is coupled to further provide the negative voltage and the negative control voltage to a second decoder coupled to another wordline of the memory array.